Notice of References Cited	Application/Control No. 10/040,122	Applicant(s)/Patent Under Reexamination SCOTT ET AL.		
	Examiner Leigh Marie Garbowski	Art Unit 2825	Page 1 of 3	

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-6,363,519 B1	03-2002	Levi et al.	716/16
	B	US-5,805,795	09-1998	Whitten, Thomas G.	714/38
	C	US-5,774,358	06-1998	Shrote, Curtis K.	700/86
	D	US-5,708,774	01-1998	Boden, Edward Barnes	714/38
	E	US-5,703,789	12-1997	Beausang et al.	716/4
	F	US-5,455,938	10-1995	Ahmed, Sultan	716/5
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Goldstein, "Controllability/Observability Analysis of Digital Circuits," IEEE Trans. on Circuits and Systems, Vol. CAS-26, No. 9, September 1979, pages 685-693.
	V	Saab et al., "CRIS: A Test Cultivation Program for Sequential VLSI Circuits," 1992 IEEE/ACM Int'l Conference on Computer-Aided Design, pages 216-219.
	W	Rudnick et al., "A Genetic Approach to Test Application Time Reduction for Full Scan and Partial Scan Circuits," 8th Int'l Conference on VLSI Design, January 1995, pages 288-293.
	X	O'Dare et al., "System design for test using a genetically based hierarchical ATPG system," 1995 IEE Colloquium on Systems Design for Testability, pages 9/1-9/5.

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-			
	B	US-			
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Ravikumar et al., "Synthesis of Testable Pipelined Datapaths using Genetic Search," 9th Int'l Conference on VLSI Design, January 1996, pages 205-210.
	V	Corno et al., "GATTO: A Genetic Algorithm for Automatic Test Pattern Generation for Large Synchronous Sequential Circuits," IEEE Trans. on CAD of ICs and Systems, Vol. 15, No. 8, August 1996, pages 991-1000.
	W	Rudnick et al., "A Genetic Algorithm Framework for Test Generation," IEEE Trans. on CAD of ICs and Systems, Vol. 16, No. 9, September 1997, pages 1034-1044.
	X	Chiusano et al., "RT-level TPG exploiting high-level synthesis information," 1999 Proc. VLSI Test Symposium, pages 341-346.

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

		Notice of References Cited		

Application/Control No.	Applicant(s)/Patent Under Reexamination
10/040,122	SCOTT ET AL.

Examiner	Art Unit	
Leigh Marie Garbowski	2825	Page 3 of 3

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-			
	B	US-			
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Xu et al., "An evaluation of test generation algorithms for combinational circuits," 1999 Proc. East Asian Test Symposium, pages 63-69.
	V	Shen, "Genetic algorithm based test generation for sequential circuits," 1999 Proc. East Asian Test Symposium, pages 179-184.
	W	Xu et al., "Forecasting the Efficiency of Test Generation Algorithms for Digital Circuits," 2000 Proc. 9th Asian Test Symposium, pages 179-183.
	X	Harmanani et al., "A genetic algorithm for testable data path synthesis," 2001 Canadian Conference on Electrical and Computer Engineering, pages 1073-1078.

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.